

# Treegion Scheduling for Wide Issue Processors

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## Abstract

Instruction scheduling is one of the most important phases of compilation for high-performance processors. A compiler typically divides a program into multiple regions of code and then schedules each region. Many past efforts have focused on *linear* regions such as traces and superblocks. The linearity of these regions can limit speculation, leading to under-utilization of processor resources, especially on wide-issue machines. A type of *non-linear* region called a *treegion* is presented in this paper. The formation and scheduling of treeregions takes into account multiple execution paths, and the larger scope of treeregions allows more speculation, leading to higher utilization and better performance. Multiple scheduling heuristics for treeregions are compared against scheduling for several types of linear regions. Empirical results illustrate that instruction scheduling using treeregions — *treegion scheduling* — holds promise. Treegion scheduling using the *global weight* heuristic outperforms the next highest performing region — superblocks — by up to 20%.

## 1 Introduction

Contemporary high performance microprocessors detect and extract instruction-level parallelism (ILP) by using a combination of hardware and compiler techniques. Within the compiler, instruction scheduling is a phase that can play a key role in exploiting ILP. A compiler typically divides a program into multiple *regions*, areas of code that tend to execute together, and then schedules each region.

Many past efforts have focused on *linear* regions, that is, regions which contain one control path. Trace scheduling [1] forms regions in which the basic blocks of each region, called a trace, may execute in order

from top to bottom. Superblock scheduling [2] forms superblocks, regions with a single entrance and (possibly) multiple exits. Both of these techniques use profile information to guide the region formation process [3], so that the most often executed paths reap the greatest benefit.

The linearity of these regions and their dependence on profile information can be detrimental to performance under some conditions. The actual execution patterns of a program may vary from the predictions inferred from profile information, which can cause a reduction in program performance [4], [5]. Also, restricting regions to linear sets of basic blocks intrinsically limits speculation and can lead to under-utilization of processor resources, especially on wide-issue machines. An additional complexity of traces is the presence of *merge points*, basic blocks which have multiple incoming control flow edges. The use of speculative execution in this case requires special care such as bookkeeping code, which consumes machine resources and adds more complexity to the compiler.

This study presents an analysis of a *non-linear* region called a *treegion*. A treegion encompasses a decision-tree subgraph of a program's control flow graph (CFG). Treegion formation is performed without profile information, and instruction scheduling across a treegion — a process that is termed *treegion scheduling* — can use or ignore this information. Both processes take into account multiple execution paths, not just a single one. The larger scope of treeregions gives the scheduler more chances to speculate operations, leaving less idle resources. Since they are tree structures, the complexity of merge points is avoided as well. This study builds upon our earlier work in treegion scheduling [6], [7].

This paper is organized as follows. Section 2 defines a treegion and describes the treegion formation process. Section 3 introduces treegion scheduling and several heuristics that can be applied to the process. Section 4 shows how tail duplication during treegion

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formation and the use of *dominator parallelism* during scheduling can improve the performance of tree-region schedules. Section 5 reviews related work in non-linear regions, and Section 6 concludes the paper.

## 2 Tree-region Formation

The tree-region is named for the fact that it is a region containing a tree of basic blocks which is a subgraph of the CFG of a program. Therefore, formation of a tree-region is dependent only on the CFG topology. A tree-region can contain multiple, independent control paths that diverge from the *root* (block) of the tree. Since it is a tree, a tree-region is acyclic and contains no merge points except possibly the root itself.

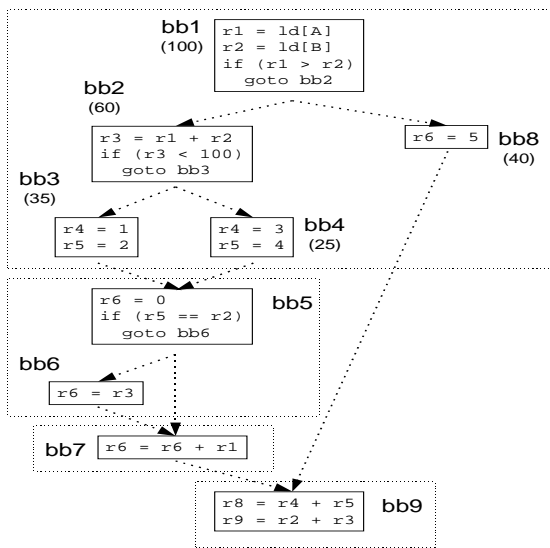


Figure 1: A CFG divided into tree-regions.

Figure 1 shows a CFG after tree-region formation, where each tree-region is surrounded by dotted lines. Note that some tree-regions contain only one basic block, while others contain several. The tree-region formation algorithm is shown in Figure 2. Tree-regions are grown across a CFG starting from the entry points, each of which roots a new tree-region. From a given root, the CFG is traversed, and basic blocks are absorbed into the root’s tree-region if they are not merge points. Eventually, only merge points remain following a tree-region’s leaf blocks. These are called *saplings* of the tree-region and become the roots of new tree-regions. The process continues until the entire CFG has been consumed, at which time each basic block is in exactly one tree-region.

The programs of the SPECint95 benchmark suite were run through the tree-region formation process. The programs had classic optimizations and a profiling

```

1 treeform (CFG)
2 {
3   Add top node(s) of CFG to unprocessed queue
4   while unprocessed queue is not empty {
5     Get first node in unprocessed list
6     if node is already in a tree-region continue
7
8     Make a new empty tree-region
9     absorb-into-tree (tree-region, node)
10
11    for each sapling of current tree-region
12      if sapling is not in a tree-region
13        add sapling node to unprocessed queue
14  }
15 }
16 absorb-into-tree (tree-region, node)
17 {
18   Add node to candidate queue
19   while candidate queue is not empty {
20     Get first node in candidate queue
21     if node is already in tree-region continue
22     if node is a merge point and not the root
23       continue
24
25     Move node into tree-region
26     Add each successor of node to (front of)
27     candidate queue
28   }
29 }
  
```

Figure 2: Tree-region formation algorithm. The first algorithm, *treeform*, builds tree-regions over an entire CFG. The second, *absorb-into-tree*, adds nodes starting from the one given into the tree-region.

run using training inputs applied to them using the IMPACT compiler [2]. The benchmarks were then converted to the Rebel textual intermediate representation by the Elcor compiler from Hewlett-Packard Laboratories [8]. Region formation was performed using the LEGO compiler, a research compiler developed at N.C. State University [6]. The results are tabulated in Table 1. The average tree-region in SPECint95 contains two to four basic blocks and between 20 and 25 instructions. Tree-regions clearly contain more operations than basic blocks and thus can enable the extraction of high levels of ILP.

## 3 Tree-region Scheduling

The motivation for building tree-regions is the ability to schedule multiple execution paths simultaneously. This provides more opportunity for speculation and also allows the scheduler to better balance the needs of the different paths.

The speculative hedge heuristic [4] inspired many of the particulars of tree-region scheduling. This technique provides various ways to prioritize instructions in superblocks, based on the weights of the exits they precede, the number of exits they precede, and other factors. The goal of speculative hedge is to avoid delaying execution paths even if they do not execute fre-

Program	avg # bb	max # bb	avg # instrs
compress	2.43	8	17.63
gcc	2.85	384	21.54
go	2.75	89	20.95
ijpeg	2.39	69	20.87
li	2.56	44	18.29
m88ksim	3.38	146	25.68
perl	3.14	774	23.45
vortex	3.30	39	33.53

Table 1: Treeregion statistics. The data presented, from left to right, are average basic block count per treeregion, maximum basic block count in a treeregion, and average number of operations per treeregion.

quently; the ideas presented in this technique adapt nicely to treeregion scheduling.

First, treeregion scheduling will be described, and an example will be presented which shows how treeregion scheduling can produce a more efficient schedule than superblock scheduling. Then, the results of experiments using four different treeregion scheduling heuristics will be presented.

### Basic treeregion scheduling algorithm

```

1 scheduleTreeregion (treeregion)
2 {
3   Form DDG for treeregion
4   sortDDGNodesBy*** (DDG)
5   listSchedule (DDG)
6 }
```

Figure 3: Treeregion scheduling algorithm. The sort function can be replaced with various sorting schemes, each representing a different heuristic.

Figure 3 shows the basic treeregion scheduling algorithm. The first step of the three-step process is the construction of a data dependence graph (DDG) for the treeregion being scheduled. The second step is the sorting of the nodes in the DDG into a list for the third step, list scheduling. The sort function directly affects the quality of the schedules produced, and the heuristics presented in the rest of this section vary in how they perform this sorting.

Because the DDG may contain instructions from separate paths, the list scheduler may place instructions from multiple paths into the same cycle in the schedule. If the instructions do not conflict in their use and/or definition of data items, this causes no problems. If they do conflict, compile-time register

renaming [9] is used.

The treeregion scheduler can speculate instructions above branches. Speculating an instruction above a branch may cause incorrect execution if the instruction defines data that is used on another exit from the branch. The treeregion scheduler uses register renaming to prevent such live-out violations.

The treeregion scheduler often produces schedules where several branches are scheduled in one cycle (providing the architecture allows it). Predication [10] is used to ensure that the proper branch is executed. The combination of predicated branches and speculation is similar to techniques used for critical path reduction [11].

Unit 0	Unit 1	Unit 2	Unit 3
<i>r1 = LD (A)</i>	<i>r2 = LD (B)</i>	<i>b8 = PBR (bb8)</i>	<i>b4 = PBR (bb4)</i>
<i>p1 = CMPP (r1&gt;r2)</i>	<i>r3 = r1 + r2</i>	<i>b5 = PBR (bb5)</i>	<i>r4 = 1</i>
<i>BRCF (b8, p1)</i>	<i>p3 = CMPP (r3&lt;100)</i>		
<i>BRCF (b4, p3)</i>	<i>r5 = 2</i>		
<i>BRU (b5)</i>			
<b>bb4: r4 = 3</b>	<i>r5 = 4</i>	<i>b5 = PBR (bb5)</i>	
<i>BRU (b5)</i>			
<b>bb8: r6 = 5</b>	<i>b9 = PBR (bb9)</i>		
<i>BRU (b9)</i>			
execution time = 35(5) + 25(6) + 40(5) = 525			

Figure 4: An example superblock schedule. Instructions in italics are speculated above branches upon which they are dependent.

Figures 4 and 5 show schedules for the topmost treeregion in Figure 1 using superblock scheduling and treeregion scheduling, respectively<sup>1</sup>. The estimated execution times for both schedules are derived by multiplying the schedule height of each path by the number of times the profile weights indicate that the path will be executed. A four-issue processor with universal functional units and unit instruction latencies is assumed. The schedules use operations similar to those found in Hewlett-Packard Laboratories Play-Doh specification [12] that are also common in other experimental architectures: speculation, predication, and a compare-to-predicate operation. Registers beginning with “r” are general-purpose integer registers, those beginning with “p” are predicate registers, and those beginning with “b” are branch target registers (BTRs). The PBR operation initializes a BTR by

<sup>1</sup>For simplicity, the examples only consider the topmost treeregion.

Unit 0	Unit 1	Unit 2	Unit 3
<i>r1 = LD (A)</i>	<i>r2 = LD (B)</i>	<i>b2 = PBR (bb2)</i>	<i>b3 = PBR (bb3)</i>
<i>p1, p2 = CMPP(r1&gt;r2)</i>	<i>r3 = r1 + r2</i>	<i>b5 = PBR (bb5)</i>	<i>b6 = PBR (bb5)</i>
BRCT (b2, p1)	<i>p3, p4 = CMPP(r3&lt;100) ? p1</i>	<i>b9 = PBR (bb9)</i>	<i>r4 = 1</i>
<b>bb2</b> : BRCT (b3, p3)	<i>r5 = 2</i>	<i>r4a = 3</i>	<i>r5a = 4</i>
<b>bb3</b> : r6 = 5	BRCT (b5, p3)	BRCT (b6, p4)	BRCT (b9, p2)
execution time = 35(5) + 25(5) + 40(5) = 500			

Figure 5: An example treegion schedule. Instructions in italics are speculated above branches upon which they are dependent. Instructions in shaded blocks show the effect of register renaming.

setting it to a target address, the CMPP operation saves the result (and optionally, the complement of the result) of a comparison into destination predicate registers, and the BRCT, BRCF, and BRU operations are branches if condition true, if condition false, and unconditionally, respectively.

The superblock schedule (Figure 4) is split into three sections. The top section is for the superblock created from (bb1, bb2, bb3), the middle section is for bb4, and the bottom section is for bb8. The estimated execution time for this section of code is 525 cycles. The treegion schedule (Figure 5) executes in 500 cycles, 25 less than the superblock schedule. This is primarily due to the speculation of additional instructions from bb4.

On a very wide machine, both schedulers are able to speculate more instructions. However, the treegion scheduler has access to multiple paths, allowing even more speculation and facilitating the completion of additional paths.

Note that the first operation in the fifth cycle of the treegion schedule ( $r6 = 5$ ) is executed unconditionally instead of being predicated. This is permissible since  $r6$  is not live-out on any paths out of the treegion, so no conflicts arise. If  $r6$  were live-out, register renaming can be used as described above.

The different scheduling heuristics presented in the remainder of this section are compared with basic block scheduling and with scheduling for *simple linear regions* (SLRs). Simple linear regions are formed in the same manner as superblocks, but tail duplication is not permitted. In fact, their formation is implemented as a special case of treegion formation, where for a given node (basic block) placed into an SLR,

Program	avg # bb	max # bb	avg # Ops
compress	1.30	3	9.43
gcc	1.26	54	8.98
go	1.20	22	9.16
jpeg	1.32	18	11.58
li	1.44	7	10.25
m88ksim	1.34	9	10.19
perl	1.27	24	9.29
vortex	1.25	8	12.71

Table 2: SLR statistics. The data presented above, from left to right, are average basic block count per SLR, maximum basic block count in an SLR, and average number of operations per SLR.

the successor node with the highest profile weight is selected next for possible inclusion rather than all successors of the node. The result is a single-entry, multiple-exit region formed without tail duplication. Treegions will be compared with superblocks in Section 4, after the application of tail duplication to treegions has been presented.

Characteristics for the regions resulting from SLR formation across SPECint95 are presented in Table 2. The SLRs typically include 1-2 basic blocks and 8-12 instructions, which is less than treegions formed over the same programs. Tables 1 and 2 illustrate that a treegion provides a scheduler with more instructions (as well as more paths) to speculate and schedule.

Before presenting the heuristics used for treegion scheduling and the results, our framework for these experiments will be described. Programs from the SPECint95 benchmark suite were used, as explained in Section 2. Two machine models were used for this study: a 4-issue processor (4U) and a 8-issue processor (8U), both with universal units. Both machines are statically-scheduled, very long instruction word (VLIW) architectures [1] (A VLIW instruction can also be referred to as a *MultiOp*, with each individual operation in the MultiOp termed an Op [13]. The Op/MultiOp terminology is used in the remainder of this paper.) All operations in the two machines are unit latency except for load (2 cycles), floating-point multiply (3 cycles), and floating-point divide (9 cycles). Memory operations are serialized (loads cannot bypass stores) since no aliasing information is available, and since the machine models are Playdoh-style machines a store and any dependent memory operations can be scheduled in the same cycle. All functional units are fully pipelined. Program performance was measured by using the profile count and schedule height of each region to estimate execution time. The effects of instruction and data caches were ignored,

and perfect branch prediction was assumed, in order to determine the maximum benefit of the scheduling heuristics. Speedup over basic block scheduling on a single-issue, pipelined universal unit machine was the performance metric used. Copy Ops added due to renaming were not used in computing speedup.

### Dependence height treeregion scheduling

The dependence height heuristic — also commonly referred to as critical path scheduling — is the simplest of the heuristics discussed here. In the second step of treeregion scheduling, the DDG nodes are sorted by their heights. This provides the most opportunity for speculation since Ops very far down in the treeregion that have a large dependence height are given the same priority as those nearer the treeregion root. On a very wide machine a large amount of speculation will occur due to abundant processor resources.

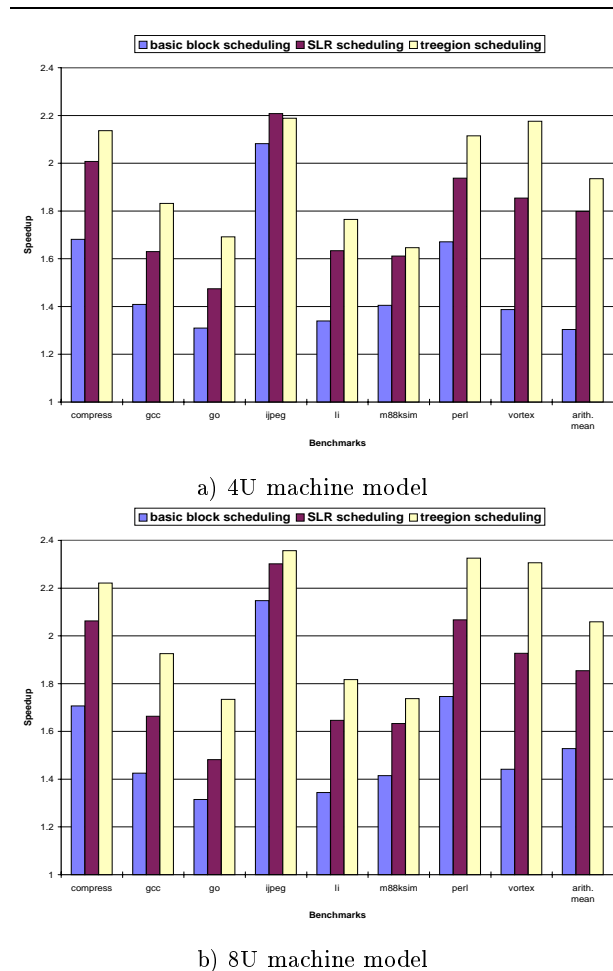


Figure 6: Dependence height treeregion scheduling.

The results of the experiments with dependence

height treeregion scheduling are shown in Figure 6.

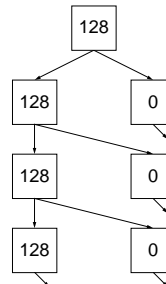


Figure 7: A biased treeregion. The block numbers indicate profile weight. The leftmost path is the only path executed in the treeregion.

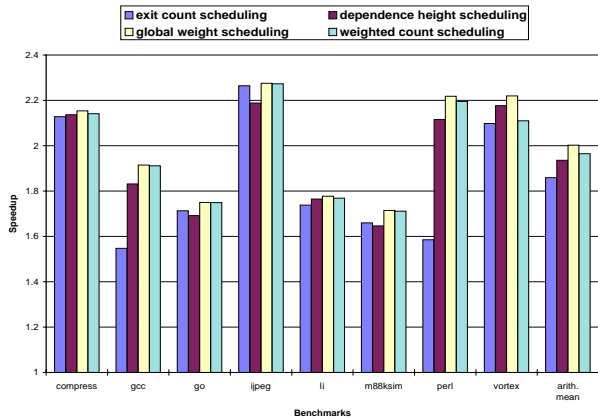
The results show that this heuristic performs well. The speedup for treeregion scheduling here exceeds that of ordinary basic block scheduling by 48% and 35% for the 4U and 8U machine models, respectively, and it also exceeds the speedup of SLR scheduling by 8% and 11% (SLR scheduling was performed as treeregion scheduling using the dependence height heuristic as well). The speedup for treeregion scheduling is always the greatest except for the 4U schedule for *jpeg*; this is because that particular benchmark has a preponderance of *biased* treeregions, where a single path is executed 100% of the time. An example of such a treeregion in *jpeg* is shown in Figure 7. SLRs can focus on this path by itself, while treeregions allow their schedule heights to stretch a bit in order to give several paths a chance to execute.

Though the results for this heuristic at first seem promising, there is a danger of overaggressive speculation for heavily-executed large treeregions. Exits from these treeregions may be delayed because Ops from less frequently executed paths which happen to have a greater dependence height may be speculated into the top of the treeregion schedule. This would lead to poor usage of resources since the results of these speculated Ops are rarely used while all execution paths in the treeregion are delayed. The next heuristic attempts to avoid this danger.

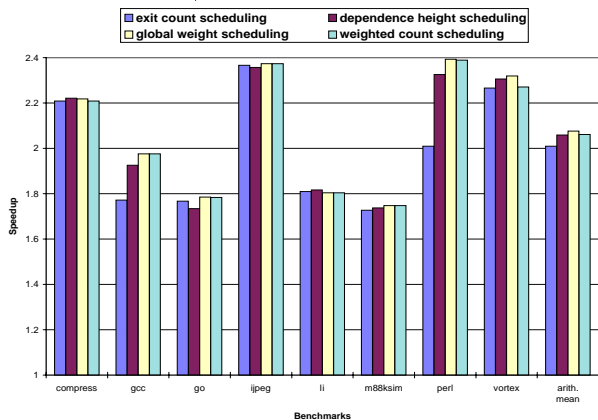
### Exit count treeregion scheduling

The scheduling results for the remaining three heuristics are presented in Figure 8. Each heuristic will be described in turn, accompanied by an analysis of the heuristic’s results.

The exit count heuristic is adapted from the helped count priority function of speculative hedge [4]. In



a) 4U machine model



b) 8U machine model

Figure 8: The four treregion scheduling heuristics.

this scheme, the priority of an Op is equal to the Op’s *exit count*, which is the number of exits that follow the Op in control flow in the treregion. This heuristic gives highest priority to Ops in the root of the treregion, since by definition they help every exit in the treregion. The nodes in the treregion DDG are sorted first by exit count; then, Ops with the same exit count are sorted by dependence height.

This heuristic attempts to curtail any overaggressive speculation by accounting for the treregion topology; however, the results are mixed, and overall the dependence height heuristic provides 2–4% higher speedup. Notably, this heuristic performs very poorly on **gcc** and **perl**.

An explanation for the surprising results for the exit count heuristic was found by examining particular treregions in the two problem benchmarks. These treregions were each rooted by a very wide multiway branch, and their leaves were the various choices for the branches. Furthermore, the treregions were shal-

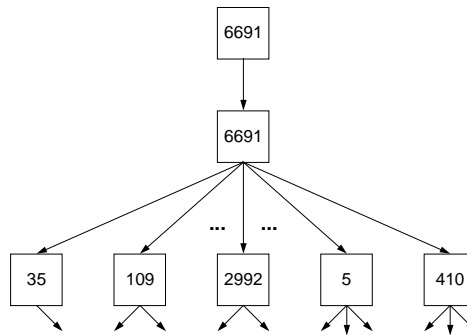


Figure 9: A wide, shallow treregion. The block numbers indicate profile weight. The branch destinations with the highest exit count are not necessarily the most often executed.

low; only a few treregion exits resided along any one branch destination. A simplified example of such a treregion, taken from **gcc**, is shown in Figure 9.

The fundamental flaw of the exit count heuristic exposed by these treregions is the assumption that an area of code with a higher exit count typically has a higher profile weight. In these treregions, each area of code at a branch destination had a roughly equal (small) exit count. However, most of them (not shown) had zero profile weight, and those with the highest exit counts did not have the highest weight.

As a result of this flaw, those branch destinations with low exit count and high profile weight were given less priority than those with a high exit count but a low profile weight. The most often executed sections of the treregion away from the root were therefore delayed. This behavior was aggravated by the large width and symmetry of the treregions. On the other hand, the dependence height heuristic is more democratic in these situations, and tends to schedule all destinations at an equal priority. Hence it produces better schedules for these treregions.

### Global weight treregion scheduling

The global weight heuristic uses profile weights to prioritize Ops. This gives an advantage to Ops executed more often, which may help the most frequently executed paths be scheduled more quickly. The priority value assigned to an Op is the profile weight of the original basic block which contains it. Ops with the same weight are sorted by dependence height. This heuristic stems from the helped weight heuristic of speculative hedge, which uses the total weight of all exits helped by an Op as a priority value. Since a tree-

gion is fundamentally a tree of execution paths, the weight of all exits reached through an Op in a treegion is equal to the weight of that Op’s basic block.

The results in Figure 8 show that this heuristic has the best overall performance. It provides 3% higher speedup than the dependence height heuristic for the 4U machine model, and about 1% higher speedup for the 8U model. There is greater improvement for the 4U model because the global weight heuristic targets heavily executed Ops aggressively, and this tactic pays off more when resources are less available.

Note that the global weight heuristic avoids the flaw of the exit count heuristic, at the expense of relying on profile information. By targeting those areas of code with high weight, the global weight heuristic selects the proper branch destinations of the multi-way branches and gives them highest priority.

### Weighted count treegion scheduling

The weighted count heuristic combines the global weight and exit count heuristics. The focus on profile weight of the former heuristic is tempered by the restrictions on speculation imposed by the latter. The primary sorting criterion is profile weight, to give heavily executed Ops an advantage. Ops with the same weight are sorted by exit count to avoid overaggressive speculation. Ops with both the same weight and exit count are sorted by dependence height.

The hope for this heuristic is that the flaw in the exit count heuristic will be avoided by prioritizing Ops primarily by weight. However, it does not improve over the dependence height heuristic as much as the simpler global weight heuristic. In particular, the speedup of **vortex** is reduced.

The reason for the slight degradation in performance is again due to sorting by exit count. By giving highest priority to Ops early in a treegion, the heuristic naturally retires exits higher in the treegion earlier. However, the most taken exits may be lower in the treegion, and thus are delayed. The sorting by weight that the weighted count heuristic performs partially solves this problem, but when the weights in a treegion are equal or very close, and the exits near the bottom are taken most often, the performance degradation surfaces.

This effect is most noticeable in biased treegions that are also *linearized*, i.e., that contain a single execution path. An example of a linearized treegion in **vortex** is shown in Figure 10. Since the weights of the blocks are the same, the weighted count heuristic behaves like the exit count heuristic, and so the only taken exit at the bottom of the treegion is delayed. On the other hand, the global weight heuristic treats

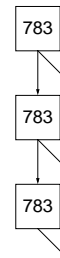


Figure 10: A linearized treegion. The block numbers indicate profile weight. The most frequently taken exit is at the bottom of the treegion; the weighted count heuristic instead focuses on the intermediate exits, which are never taken.

all of the blocks equally, and manages to schedule the taken exit in less time.

In summary, the dependence height and global weight heuristics produce the best overall speedup. The former heuristic is useful when profile information is unavailable or unreliable, while the latter can make use of reliable profile information. The exit count and weighted count heuristics suffers from some flaws; however, it remains to be seen whether they perform well in the face of profile variations, where they may preserve performance better.

## 4 Applying Tail Duplication to Treegions

Intuition suggests that large treegions are better for producing high-performance schedules than small treegions, since large treegions provide more opportunity for speculation. This section examines the use of tail duplication in expanding treegions and compares the schedules derived from them with superblocks.

### Tail duplication heuristics

The fundamental goal of any attempt to expand treegions beyond their normal size is to eliminate merge points, since they delimit treegion boundaries. Tail duplication, a process applied during superblock [2] and hyperblock [14] formation, can be used in treegion formation to convert saplings (which are merge points) into a set of single entry blocks which can be absorbed into surrounding treegions. Before describing the algorithm for treegion formation with tail duplication, the heuristics applied to tail duplication will be described.

A code expansion limit is the primary heuristic. Uncontrolled code expansion will create large treeregions at the expense of treeregions following them in the code. Limiting code expansion creates more balanced treeregions and keeps the code size and compile time under control. The number of distinct execution paths in a treeregion (*path count*) is also limited for similar reasons. A large number of paths in a treeregion will lead to increased interference between paths when competing for schedule slots, so limiting their number prevents some from being delayed too long.

Finally, a limit on a tail duplicated sapling's *merge count*, or number of incoming edges, is used. Tail duplicating a sapling with a large merge count is expensive in terms of code size and compile time. Therefore, saplings with high merge counts are not tail duplicated unless they are merge points with no successors in the CFG, such as function exits.

### Modified treeregion formation algorithm

---

```

1 treeregion-td (CFG)
2 {
3   Add top node(s) of CFG to unprocessed queue
4   while unprocessed queue is not empty {
5     Get first node in unprocessed list
6     if node is already in a treeregion continue
7     Make a new empty treeregion
8     absorb-into-tree (treeregion, node)
9     do {
10      if treeregion path count exceeds limit break
11      for each sapling of current treeregion {
12        if sapling is in another treeregion
13          continue
14        if code expansion limit might be exceeded
15          continue
16        if sapling merge count exceeds allowed
17          limit continue
18        use this sapling
19      }
20      if sapling selected for tail duplication {
21        if sapling is merge point
22          tail-duplicate (sapling onto node
23                        in tree)
24        absorb-into-tree (treeregion, duplicate)
25      } else
26        absorb-into-tree (treeregion, sapling)
27    }
28  } while some sapling is selected for tail
29  duplication
30  for each sapling of current treeregion
31    if sapling is not in a treeregion
32      add sapling node to unprocessed queue
33  }
34 }

```

---

Figure 11: Treeregion formation algorithm with tail duplication. After the initial formation, tail duplication is performed and duplicates are added to the treeregion until no saplings can be tail duplicated.

The treeregion formation algorithm can be modified to use tail duplication; the result is shown in Figure 11. Tail duplication is performed on each treeregion as it is formed, before the next treeregion is created. A sapling which qualifies is found and tail duplicated. The duplicate is then absorbed into the treeregion. This continues until no qualifying saplings remain. Often a sapling that has been tail duplicated will have only one remaining incoming edge. The algorithm takes this into account and absorbs such saplings directly.

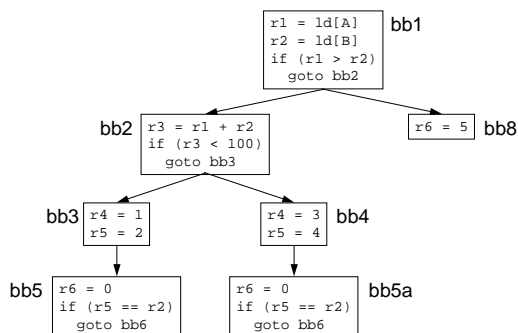


Figure 12: A treeregion after tail duplication. The top-most treeregion in Figure 1 is shown above after bb5 has been tail duplicated.

Figure 12 shows the topmost treeregion of Figure 1 after basic block 5, originally a merge point, has been tail duplicated, and both the original block and its duplicate have been absorbed into the treeregion. This process could be continued through the CFG in Figure 1 to the leaf node at basic block 9, resulting in one large treeregion where each execution path through the original CFG has been converted into a unique path through the treeregion. The entire CFG could then be scheduled as a single unit.

### Dominator parallelism in treeregion scheduling

A primary drawback of tail duplication is the introduction of redundant operations which may waste resources and extend execution time when speculated. In some cases the scheduler can take advantage of *dominator parallelism* to eliminate redundant Ops from the schedule.

Dominator parallelism is exhibited by identical Ops from different execution paths which are speculated into a block that dominates each Op [15]. When this occurs, all but one of the Ops can be safely eliminated from the schedule. The remaining Op will perform



the operation for all paths concerned. The Op often is still speculative, as varying data dependencies may have prevented identical Ops from *all* paths from being speculated into a single dominator, but when a complete set of identical Ops has moved into a dominator, the single Op can be made non-speculative. Dominator parallelism has been used and discussed in both research and commercial contexts [16], [17].

The treegion scheduler can easily detect dominator parallelism between tail duplicated Ops. Because of the treegion’s structure, any block in a treegion dominates all blocks below it. Ops speculated upwards are always speculated into dominators. Therefore, if a tail duplicated Op  $A'$  is speculated into a block where one of its duplicates  $A''$  is already scheduled,  $A'$  can be eliminated.

As a simple example, refer to basic blocks 5 and 5a in Figure 12. The operation  $r6 = 0$  in both blocks may be speculated into basic block 2 (or 1). If this occurs, then only one copy of the Op needs to be scheduled and the work will be done for both execution paths.

### Comparison with superblocks

Experiments were run to show the effects of tail duplication and dominator parallelism on treegion scheduling. The results are compared to superblock scheduling<sup>2</sup>. In these experiments, the code expansion limit is set to 2.0 and 3.0 times the original code size per treegion. The merge count limit is held at four and the path count limit at twenty.

Tables 3 and 4 present statistics on the characteristics of the superblocks and treegions with tail duplication formed by the LEGO compiler. Figure 4 shows the sizes of the regions formed. For most of the programs, treegions contain more basic blocks and Ops than superblocks. This is an intuitive result, since treegions consider multiple paths. Table 4 shows the amount of code expansion that occurs when forming superblocks and treegions. Treegions experience more code expansion than superblocks, another intuitive result, since tail duplication can occur along multiple paths within a treegion. Overall, the amount of code duplication is moderate for both types of regions. This implies that the instruction cache behavior of the programs will not be dramatically affected by the increase in code size.

Figure 13 shows the results of treegion scheduling using the global weight heuristic versus superblock

<sup>2</sup>Every attempt was made to produce superblocks within the LEGO compiler as described in the literature [2], [18], [19]; differences between the LEGO compiler and the IMPACT compiler are unavoidable, but minimized.

Program	Region type		
	sb	tree (2.0)	tree (3.0)
compress	1.26	1.34	1.62
gcc	1.14	1.32	1.43
go	1.21	1.33	1.40
jpeg	1.15	1.26	1.38
li	1.20	1.26	1.31
m88ksim	1.19	1.34	1.49
perl	1.07	1.30	1.38
vortex	1.17	1.37	1.45
average	1.18	1.32	1.44

Table 3: Code expansion statistics. The data presented indicate the factor by which code size increased for superblocks (sb) and treegions (tree). The numbers in parentheses indicate treegion code expansion limits.

scheduling. For both machine models, the speedup of treegion scheduling exceeds that of superblock scheduling by 15% with a code expansion limit of 2.0 (actual code expansion 1.32), and by 20% with a code expansion limit of 3.0 (actual code expansion 1.44). Overall, just as with treegions without tail duplication versus SLRs, the additional paths and Ops available within a treegion enable the extraction of higher levels of ILP.

## 5 Related work

Previous work on non-linear regions have influenced the study of treegions. The most direct ancestor to this work is decision tree scheduling (DTS) [20]. DTS recurses down the paths of a decision tree (similar to a treegion) producing schedules. Guarded instructions, the predecessors of predicated instructions [10], occupy branch delay slots. Ops are prioritized by the weight of the execution paths running through them and by their position along the critical path, a heuristic similar to global weight. Although DTS shares the same spirit as treegion scheduling, the former addresses pipelined processors, while the latter is more concerned with ILP. Also, treegion scheduling has the advantage of using speculation to move operations above branches and thereby exploiting dominator parallelism.

The IBM VLIW architecture is based on a *tree-instruction* which contains a decision-tree set of operations. The machine evaluates the various conditionals and executes all necessary operations in a single cycle. The finite-resource global scheduling technique [21] schedules ordinary code into tree-

Benchmark	Region type					
	# regions		avg # bb		avg # Ops	
	sb	tree (2.0)	sb	tree (2.0)	sb	tree (2.0)
compress	19	87	5.263158	5.195402	31	35.632184
gcc	3471	15186	5.576491	6.152575	32.033708	41.123864
go	1644	3280	3.753041	5.608232	24.63017	39.246646
jpeg	347	1575	3.962536	4.795556	26	37.392381
li	180	1053	4.366667	4.584995	23.7	30.91453
m88ksim	129	1483	5.844961	6.923803	72	48.937964
perl	144	3527	6.659722	6.198469	38.659722	42.955486
vortex	184	1175	9.054348	7.724255	74.945652	72.055319

Table 4: Superblock and treeregions with tail duplication statistics. The data described, from left to right, are total region count, average basic block count per region, and average number of Ops per region. 'sb' indicates a superblock, 'tree' indicates a tree.

instructions with help from a modified version of percolation scheduling [22]. The degree of speculation (DOS) heuristic controls how operations are moved through and between tree-instructions.

Hyperblocks [14] are an extension of superblocks that contain predicated code. Multiple paths are scheduled together, and predication ensures that only instructions on the taken path write back their results. Trace scheduling-2, or TRACE-2 [17], performs scheduling across a *cluster* of basic blocks. This allows the technique to detect dominator parallelism and to generate compensation code as scheduling proceeds. A speculative yield function contributes to prioritizes the operations. TRACE-2 allows merge points, but requires some scheduling complications treeregion scheduling avoids.

## 6 Conclusion

This paper presented treeregions and treeregion scheduling. A treeregion is a profile-independent tree-shaped subgraph of a program CFG. The tree topology may contain multiple paths of control. To an instruction scheduler, this presents greater opportunities for utilizing processor resources and more operations for speculative execution. The process of scheduling the operations in a treeregion is termed treeregion scheduling. Four scheduling heuristics were presented that can be used with treeregion scheduling: dependence height, exit count, global weight, and weighted count. The use of tail duplication to expand the scope of a treeregion and the exploitation of dominator parallelism to increase schedule inefficiency were also discussed. Treeregion scheduling using the various heuristics and both with and without tail duplication were compared to scheduling with three types of linear regions – basic blocks, simple linear regions, and superblocks.

The resulting performance is highly dependent on the heuristic used. The heuristic that performs best proved to be global weight, and treeregion schedules obtained with tail duplication and dominator parallelism performs 12% and 20% better than SLRs and superblocks, respectively. Based on these results, it can be concluded that treeregions are a promising alternative to more traditional, linear regions.

There are several items of interest for future work in treeregion scheduling. First, we would like to investigate the performance of treeregion schedules across different sets of inputs, to see the effects of profile variations using the various heuristics, and on dynamically scheduled processor models. Second, this study did not employ any software pipelining techniques, which would surely improve the performance of loops in the code [21]. Third, we are currently investigating the benefits of integrating code in the form of if-then and if-then-else statements into treeregions. The serialization of code using predication as in hyperblocks [14] is an alternative to using tail duplication to eliminate merge points. We also plan to compare the tradeoffs between hyperblocks and treeregions directly and to evaluate the merits of predication versus speculation for scheduling. Work on a complete implementation of hyperblocks in the LEGO compiler is currently underway.

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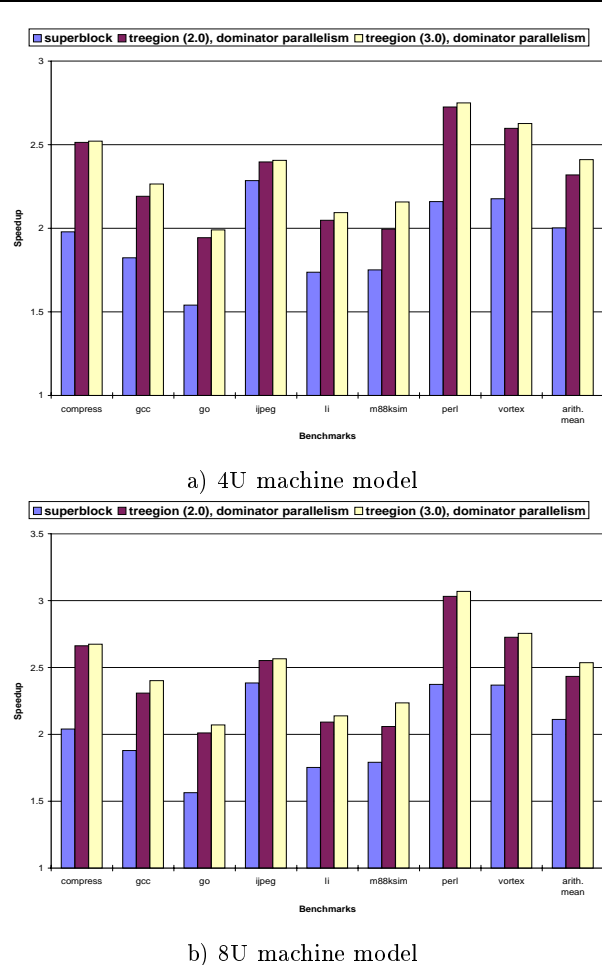


Figure 13: Results for global weight tail duplicated treeregion scheduling.

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